

CLAIMS

What is claimed:

- 1 1. A method, comprising:
2 providing a microelectronic device including an integrated circuit mounted to a
3 substrate;
4 providing a break through conductive layers of the substrate corresponding to a
5 break in power planes of the integrated circuit;
6 conducting burn-in on a first portion of the integrated circuit while a second
7 portion of the integrated circuit remains unpowered; and
8 conducting burn-in on the second portion of the integrated circuit while the first
9 portion of the integrated circuit remains unpowered.
- 1 2. The method of Claim 1 wherein providing the microelectronic device including
2 the integrated circuit mounted to the substrate further comprises providing an
3 integrated circuit with a dual core design.
- 1 3. The method of Claim 2 wherein providing the integrated circuit with the dual core
2 design does not affect the functioning of the integrated circuit.
- 1 4. The method of Claim 1 wherein providing the microelectronic device including
2 the integrated circuit mounted to the substrate further comprises providing
3 electrical connections between the integrated circuit and the substrate.

- 1 5. The method of Claim 1 wherein providing the break through the conductive layers
2 of the substrate corresponding to the break in the power planes of the integrated
3 circuit enables the burn-in of a first portion of the integrated circuit while a
4 second portion of the integrated circuit remains unpowered.
- 1 6. The method of Claim 1 wherein providing the break through the conductive layers
2 of the substrate corresponding to the break in the power planes of the integrated
3 circuit enables the burn-in of a second portion of the integrated circuit while a
4 first portion of the integrated circuit remains unpowered.
- 1 7. The method of Claim 1 wherein providing the break through the conductive layers
2 of the substrate corresponding to the break in the power planes of the integrated
3 circuit further comprises providing a first pin coupled to a first power supply to
4 burn-in the first portion of the integrated circuit and a second pin coupled to a
5 second power supply to burn-in the second portion of the integrated circuit.
- 1 8. The method of Claim 7 wherein providing the first pin coupled to the first power
2 supply to burn-in the first portion of the integrated circuit and the second pin
3 coupled to the second power supply to burn-in the second portion of the
4 integrated circuit comprises using circuit paths which transverse the conductive
5 layers of the substrate.
- 1 9. The method of Claim 1 further comprising heating the first portion of the
2 integrated circuit to a burn-in temperature and implementing a test voltage.

- 1 10. The method of Claim 9 further comprising initializing the first portion of the
2 integrated circuit.
- 1 11. The method of Claim 10 further comprising applying toggle patterns to the first
2 portion of the integrated circuit for a designated time.
- 1 12. The method of Claim 11 further comprising powering down the first portion of
2 the integrated circuit to burn-in the second portion of the integrated circuit.
- 1 13. The method of Claim 12 further comprising initializing the second portion of the
2 integrated circuit.
- 1 14. The method of Claim 13 further comprising applying toggle patterns to the second
2 portion of the integrated circuit for a designated time.
- 1 15. The method of Claim 14 further comprising powering down the second portion of
2 the integrated circuit.
- 1 16. A system, comprising:
2 a microelectronic device including an integrated circuit mounted to a substrate;
3 and a break through conductive layers of the substrate corresponding to a break in
4 power planes of the integrated circuit, the break through the substrate and the
5 break in the integrated circuit configured to allow rotational burn-in of the
6 integrated circuit.

1 18. The system of Claim 16 wherein the rotational burn-in includes burn-in on a first
2 portion of the integrated circuit while a second portion of the integrated circuit
3 remains unpowered and burn-in on a second portion of the integrated circuit while
4 the first portion of the integrated circuit remains unpowered.

1 19. The system of Claim 16 wherein a first pin coupled to a first power supply
2 provides power to the first portion of the integrated circuit and a second pin
3 coupled to a second power supply provides power to the second portion of the
4 integrated circuit.

1 20. The system of Claim 19 wherein the first pin and the second pin use circuit paths
2 through the conductive layers of the substrate to provide power to the first portion
3 and the second portion of the integrated circuit.

21. A system, comprising:

a microelectronic device including an integrated circuit mounted to a substrate;

a break through multiple conductive layers of the substrate corresponding to a break in the power planes of the integrated circuit, the break in the substrate and the break in the integrated circuit dividing the microelectronic device into a first portion and a second portion; and

7 a first pin coupled to a first power supply to burn-in the first portion of the
8 integrated circuit and a second pin coupled to a second power supply to burn-in
9 the second portion of the integrated circuit.

1 22. The system of Claim 21 wherein the first pin and the second pin use circuit paths
2 through the conductive layers of the substrate to provide power to the first
3 portion and the second portion of the integrated circuit.

1 23. The system of Claim 21 wherein the burn-in of the first portion of the integrated
2 circuit does not affect the second portion of the integrated circuit and the burn-in
3 of the second portion does not affect the first portion.

1 24. The system of Claim 21 wherein the integrated circuit has a dual core design
2 that does not affect the functioning of the integrated circuit.